Design of CMOS Analog Integrated Readout Circuit for NMOS THz Detectors

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***Abstract*—This paper describes design of readout circuit destined for NMOS terahertz detectors. The proposed architecture bases on chopper amplifier and instrumentation amplifier concepts. The main goals were to achieve high gain (max. 100 dB) and to enable proper operation with NMOS-based THz detector. For the research needs three different architectures of chopper amplifier have been developed. The designed chip was fabricated in well-known AMS C35 process (350 nm feature size). Another issue described in this paper is dedicated testing environment. At the end a few measurement results are shown.**

***Index Terms*—terahertz detector, chopper amplifier, instrumentation amplifier, Voltage Controlled Amplifier, Programmable Gain Amplifier, readout circuit, AMS C35.**

I. Introduction

Plasmonic field-effect transistors (FETs) have gained much attention for THz detection [1]- [3]. The use of FET as THz detector was first proposed by Dyakonov and Shur in [4]. The theory bases on analogy between the equations of the electron transport in a gated two-dimensional transistor channel and those of shallow water or acoustic waves in music instruments. A THz signal, which is applied between the source and the gate, self-rectifies by interaction of the two-dimensional electron gas (2DEG) in the transistor channel [5], the drain is typically treated as output of the detector. Electron ballistic transport enables then the FET response at the frequencies appreciably higher than the device cut-off frequency.

Design of readout circuit, which will be adjusted to FET detector response, is a complicated task. The signal originated from the detector output is a very low DC voltage (i.e. several μV). In that case the priority for readout circuit is to provide high gain and low noise. The other much-desired properties are: high input impedance and ability to control gain in a wide range. The proposed architecture of readout circuit is the chopper amplifier structure which ensures that all features mentioned above will be achieved. Moreover, in this paper the three different variants of chopper amplifier have been described. This paper addresses electrical design on the transistor-level as well as the layout issues.

The next task, described in this paper, is design of measurement application which guarantees proper stimuli generation and ability to observe the responses of the IC under test. There are many control signals which must be applied to the device under test. One should remember that designed chip contains three different architectures of readout circuit, so the number of needed signals is significant. Another important issue is design of DC voltage source of very small, adjustable amplitude. For that task special circuit with two type-J thermocouples has been used. Paper describes also several difficulties in a very low signal measurement and some solutions to overcome them.

The last part contains first results of measurements and a discussion about them. Also some further improvements of readout circuit have been proposed.

II. Chopper Amplifier

As it was written in the previous chapter, chopper amplifier architecture allows to achieve high gain and low noise level. Principle of operation of this amplifier is based on observation that it is quite easier to design a good AC voltage amplifier rather than a DC voltage one. The idea is simple: first a DC signal is modulated (e.g. by CMOS switching), next it is amplified by an AC amplifier, and - at the end - it is demodulated to a DC signal again. Diagram that explains this mechanism is shown in Fig. 1.

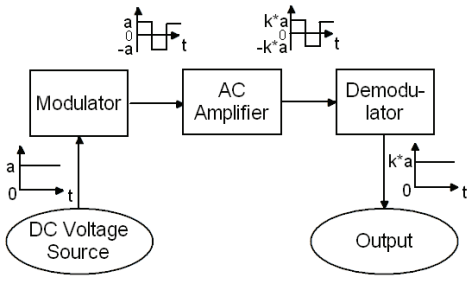

Fig. 1. The idea of chopper amplifier

The signal from DC voltage source is the input signal for circuit called modulator. Its task is to generate an AC signal of *a* amplitude from DC voltage of the value *a*. Next this signal is amplified by an AC amplifier what produces output signal of *k*a* amplitude. Finally, block called demodulator

converts this square wave into DC signal of *k*a* value. That kind of attitude has two fundamental advantages. First, it cancels the input voltage offset, because only AC component is amplified. This is the dynamic offset cancellation technique - it takes place when the amplifier is working. The second big advantage is *1/f* noise reduction. As the name suggests, it is a kind of noise which spectral power density increases with decreasing frequency. For amplification of small DC voltage signal just this type of noise dominates over the second potential source of noise in MOSFET transistors - the thermal noise. Both features mentioned above are strongly recommended for discussed readout circuit and are the main causes of choosing the chopper amplifier architecture.

A. Modulator

Modulator converts DC voltage signal of *a* value into a square wave of *a* amplitude. This is a simple task and it could be realised by basic circuit using four CMOS switches (transmission gates). This architecture is shown in Fig. 2.

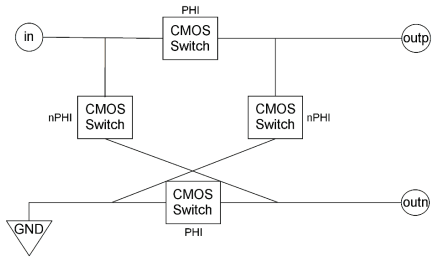

Fig. 2. Modulator's architecture

There are two pairs of switches - first of them is controlled by signal *PHI* and second one by signal *nPHI* (PHI negation). This circuit has two modes of operation: in the first one the top/bottom switches are on and the left/right are off - *in* signal appears at output *outp*, *outn* is grounded. In the second mode the situation is opposite: top/bottom switches are off, left/right are on and *in* signal appears at *outn*. The switching frequency in this case is not a critical parameter, because the input signal does not change too fast. On the other hand, it determines the f_{chop} frequency for whole chopper amplifier. Arbitrarily $f_{chop} = 1\ kHz$ has been determined, so the input signal can not change faster than 500 times per second ($f = 500\ Hz$ is the Nyquist frequency).

B. AC Amplifier

The AC amplifier amplifies square wave signal coming from modulator. Main attributes of this circuit are: high input impedance, high gain and immunity to interference. These features can be obtained in architecture called instrumentation amplifier. The scheme of this configuration is shown in Fig. 3.

The input stage, composed of two symmetric operational amplifiers, ensures high input impedance and enables simple gain control by changing the *R1*. Output stage contains

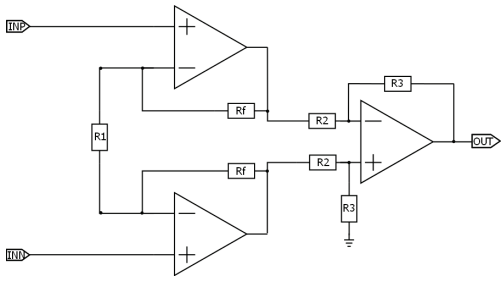

Fig. 3. Instrumentation amplifier

the operational amplifier in differential configuration. This enables to achieve the high Common Mode Rejections Ratio (CMRR), which is the tendency of the device to reject the input signals common to both input leads. It is very important because of noises contributed by CMOS switches in modulator. The gain of the amplifier is given by equation (1).

$$k_u = -\frac{R_3}{R_2}(1 + 2\frac{R_f}{R_1}) \tag{1}$$

Another desirable feature of AC amplifier is variable gain. The NMOS detector response is proportional to the intensity of THz radiation, so the ability to adjust the gain of readout circuit towards the range of input signal from the detector is very usable. There are two types of Variable Gain Amplifiers (VGA), each one has different method of gain control:

- Voltage Controlled Amplifier (VCA). This is a device that adjusts its gain in proportional manner in response to the applied control voltage signal. The control is pure analog, gain can be changed continuously.
- Programmable Gain Amplifier (PGA). This is an amplifier which gain can be controlled by external digital signals.

The concepts of VCA and PGA were utilized in some of three variants of designed readout circuit. This guarantees gain control in a very wide range.

C. Demodulator

Demodulator converts square wave signal of *a* amplitude into a DC voltage signal of *a* value. There are many different circuits which can implement this function, after analysis the sample and hold architecture has been chosen. This solution is very simple and was expected to produce good results. A scheme that shows used architecture is presented in Fig. 4.

Sample and hold circuit samples input square wave during its positive half-period and hold the value of this signal amplitude. Both of operational amplifiers are in voltage follower configuration, but they have common feedback loop. This provides low offset voltage on the output of the circuit. There are two modes of operation: sample mode and hold mode. In first of them the switch-key is closed and the input voltage

is being stored in capacitor C and appears on the output. In hold mode the switch-key is open - it disconnects capacitor from the input follower. Voltage stored in capacitor in previous mode is now held at the output. It is necessary to take care about the stability of the input follower during the hold mode - the key is open and the feedback loop of input amplifier is cut. It can be fixed by adding additional switch-keys, which close the feedback loop of the input buffer.

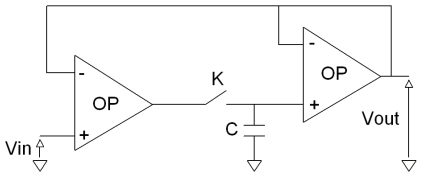

Fig. 4. Sample and hold circuit

This architecture of demodulator requires additional control signal (sample signal) which is in correlation with control signal of modulator. It was decided to generate both these signals externally rather than place this source of interferences (another switching circuits) inside the chip.

III. Readout Circuit

This section describes details related to readout circuit design. First, the architectures of folded cascode amplifier, fully differential amplifier, VCA and PGA are presented. Then all three versions of chopper amplifier are discussed. The last subsection concerns layout design.

A. Folded Cascode Amplifier

The basic operational amplifier architecture, which is used to build some more complicated structures, is based on folded cascode circuit. This one - in comparison with other amplifier architectures - provides higher gain, larger input voltage range, lower supply voltage and minimisation of Miller effect for gate-drain capacity in input transistors. Used folded cascode scheme is shown in Figure 5.

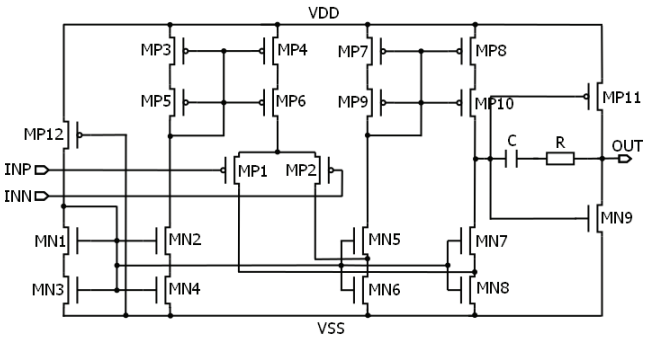

Fig. 5. Folded cascode circuit

In this circuit high precision current mirrors with four transistors have been used. High current repeatability in active load provides high gain.

B. Fully Differential Amplifier

Fully differential amplifier is a device with symmetrical inputs and symmetrical outputs. This type of amplifier requires additional circuit called Common Mode Feedback (CMFB), which controls the common mode voltage on its outputs. In single-ended operational amplifier applications the negative feedback (by connecting output to the negative input) is used and it determines dc offset (differential voltage towards ground) on the output. If device has two outputs, the common mode voltage also must be determined and this task is fulfilled by CMFB. Functional diagram of CMFB is shown at he top of Figure 6.

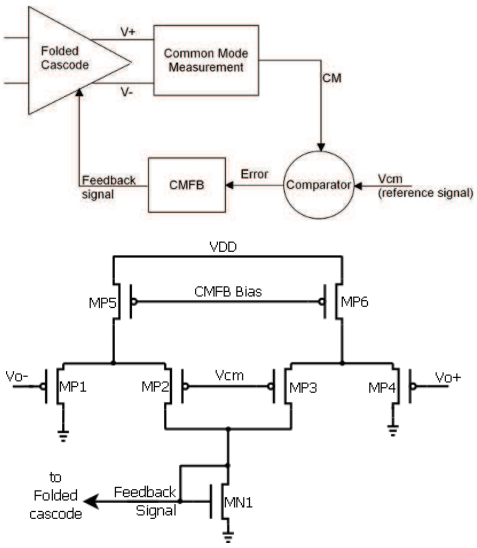

Fig. 6. Common Mode Feedback: (top) Functional diagram; (bottom) Used scheme

CMFB circuit performs three tasks: output common mode voltage measurement, comparison between this value and some reference voltage and generation of the feedback signal which controls the amplifier. Used amplifier is a folded cascode circuit (described above) with two outputs, scheme of CMFB is shown at the bottom of Figure 6.

Circuit bases on dual differential configuration, with a diode connected NMOS providing the common mode control voltage to the folded cascode circuit. With MP1-MP4 transistors matched, the current summed through MN1 is proportional to the difference between the output voltages Vo+, Vo- and a reference voltage Vcm set externally by a bias circuit. The feedback signal is used to bias the MN5-MN6 and MN7-MN8 transistors at the bottom of the folded cascode stage (see Figure 5). It is worth to notice that each one stage of amplifier needs CMFB, so circuit shown in Figure 6 is also used to bias MP11 transistor in the output stage of folded cascode.

C. Voltage Controlled Amplifier

As it was mentioned previously (in II-B), VCA is a device that adjusts its gain in proportional manner in response to

the applied control voltage signal, which can be changed continuously. Architecture of this device is based on a simple PMOS differential pair with resistive load and the relation between gain of this circuit and transistors current. The idea is shown in Figure 7.

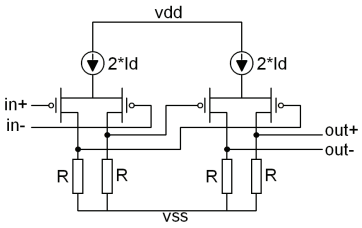

Fig. 7. The idea of VCA

The differential gain of single PMOS pair (in saturation region) with two resistors is proportional to square root of drain current, so - to achieve linear relation - combination of two differential pairs must be used (Figure 7).

To keep the transistors in saturation region it is required to limit the changes of drain currents to the proper range. Needed current source can be implemented using current mirror structure as it was shown in folded cascode (Figure 5). In the VCA circuit a resistive load is used intentionally instead of an active load. The gain of this circuit must be very low (0 dB - 20 dB range) and it can not be achieved using active load. It is also important to notice that change of drain current causes DC voltage change on the outputs. As long as the range of this changes is acceptable by application, architecture presented in Figure 7 is sufficient.

D. Programmable Gain Amplifier

As it was described in (II-B), PGA is a device which gain can be controlled by external digital signals. This can be achieved using instrumentation amplifier architecture (shown in Figure 3) with switched R1 resistor. Change of R1 influences the circuit gain according to relation (1). Modified instrumentation amplifier structure is shown in Figure 8.

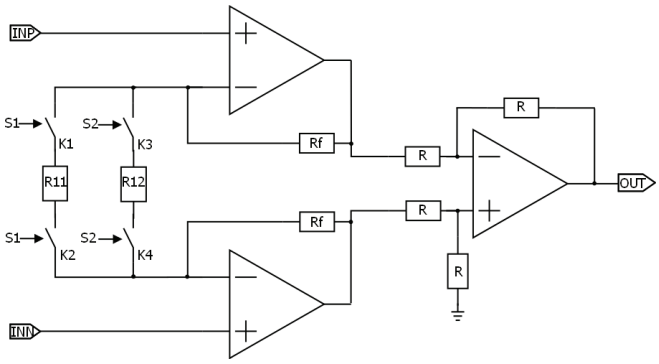

Fig. 8. Modified architecture of instrumentation amplifier

Depending on S1/S2 control signals R11/R12 resistor are attached to feedback loop, which causes the gain to be equal to 10 (20 dB) or 100 (40 dB).

E. Designed Versions of Chopper Amplifier

According to information presented before, three different versions of chopper amplifier have been designed. The difference between them concerns the AC amplifier architecture. The rest of used blocks (modulator and demodulator) are exactly the same in all three circuits. First version of AC amplifier is shown in Figure 9.

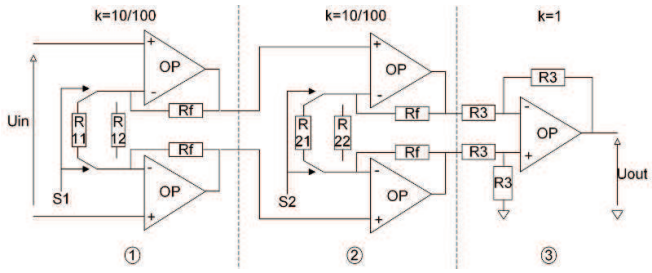

Fig. 9. First AC amplifier circuit

It is based on PGA architecture (see III-D) where the input stage has been doubled. It was done, because in single-staged circuit it is hard to achieve the high gain because of required Rf to R1 ratio (see Figure 3). According to (1) - for providing high gain - Rf value has to be very high or R1 has to be very low. Both of this solutions cause some drawbacks in IC design. High resistance can be achieved using high-resistive polysilicon layer, which is characterized by high relative variations of resistance. On the other hand, ability to use low resistances is limited by process design rules (i.e. minimum number of squares for polysilicon resistor). Using two input stages results in their gains to be multiplied (in linear scale) and it is possible to apply resistors with lower ratio of values. By means of control signals, gain of this circuit can be set to 100/1000/10000.

Second Version of AC amplifier is presented in Figure 10.

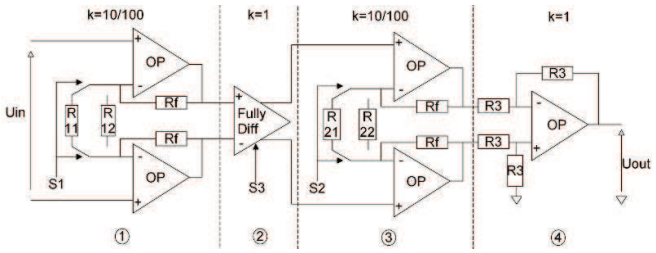

Fig. 10. Second AC amplifier circuit

It is very similar to the previous one, except that the fully differential amplifier has been placed in between fixed gain stages. This provides the ability to control common mode voltage between gain stages (by signal S3 - see III-B). It is useful when the signal with high DC component is applied to the input amplifier. Because of fact that input stage of

instrumentation amplifier transfers DC voltage component with unit gain, there is a possibility that some devices can become saturated. To avoid this, user can control common mode voltage after the first gain stage by changing signal S3. It also prevents some effects of process variations, which can affect common mode voltage.

The last, third version of AC amplifier is shown in Figure 11.

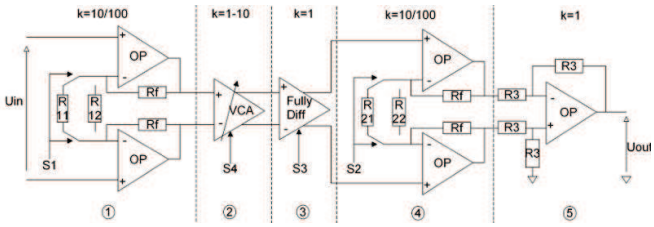

Fig. 11. Third AC amplifier circuit

In comparison with the previous one, VCA has been added. This enables linear gain control in 1-10 range using signal S4. In this circuit fully differential amplifier performs an additional function - it cancels VCA disadvantage which concerns relation between output DC component and gain value (it was mentioned in III-C). Available range of gain in this circuit is 100-100000 (40 dB - 100 dB).

F. Chip Layout

Layout of designed structure is presented in Figure 12 (2.64 X 2.64 [mm]).

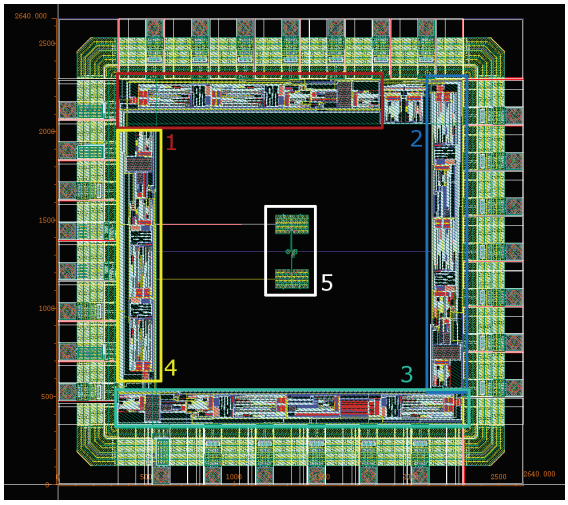

Fig. 12. Chip layout

Circuits are marked with following numbers: 1 - chopper amplifier with first version of AC amplifier, 2 - chopper amplifier with second version of AC amplifier, 3 - chopper amplifier with third version of AC amplifier, 4 - chopper amplifier with first version of AC amplifier, connected to the detector circuit, 5 - detector circuit (see chapter IV).

In this design many layout techniques have been used to achieve high immunity to interference and low susceptibility to process variations. Multifinger transistors, dummy structures, common-centroid configurations in order to reach good symmetry and minimisation of mismatches have been used. To avoid substrate coupling [6] special guard rings have been applied. The 1-4 circuits are isolated from external radiation by grounded metal 4 layer. Because of minimisation of switching noise from modulator and demodulator circuits, this devices have separate power supply and ground external pads. This prevents noise propagation by this paths.

IV. On-chip THz Detector Circuit

The prototype IC was intended to be manufactured using regular MPW run of AMS C35B4 process. It was obvious that area of silicon consumed by discussed circuits together with I/O cells and ring is significantly lower than minimum payable area in chosen run. For that reason it was decided to use the rest of silicon area to place into the chip another readout circuitry (fourth one) connected with detecting transistor equipped with antenna. The fourth readout circuit itself is a simple copy of the first variant discussed previously - as simplest and most reliable one. Because of the lack of any previous experiences concerning development of detecting circuit in chosen AMS process - on the one hand, and higher area cost of testing some collection of antennas - on the other, design of such an receiving circuit was based on extrapolation of previously examined solutions from ITE proprietary silicon process. Among all sets of NMOS + antenna one was chosen, providing maximum signal. The shape of receiving antenna was transferred in one-to-one scale, but in opposite to original solution it was created using all the four available metal layers, connected together by the via arrays. Taking into account that thicknesses of interlayer isolation are significantly lower than wave length, such "sandwich structure" can be considered as single, thicker layer. To satisfy the design rule for maximum width of metal layers it was necessary to cut them with the set of parallel slots of dimensions non visible for the THz wave. Moreover, slots in odd and even metal layers were distributed alternately. The rules of maximum slot length were satisfied by placing metal bridges within them. Another important issue was the choice of detecting transistor. During previous experiments it was observed, that maximum signal is yielded from FETs of moderate dimensions, close to process minimum, that's why it was not suitable to transfer detecting NMOS one-to-one from silicon process of nearly ten times larger feature size. On the other hand, the minimum transistor would be very hard to attach to the receiving antenna structure without narrowing the original metal paths, resulting in large parasitic inductance. Basing on these facts the NMOS of $w = 5\ \mu m$ and $l = 1.2\ \mu m$ was chosen as optimum, moreover allowing the metal path of minimum width to be placed above its gate and contacted to the polysilicon from both sides.

V. Prototypes Measurement

A. Application Board

The application board, shown in Figure 13 (top) was dedicated to prototypes measurement. It was *a priori* anticipated that due to the small input signals fed to IC under test special attention must be paid to shielding and external interferences elimination in the application board. First, the application board is supplied from 12 V/7.5 Ah rechargeable battery instead of typical power supply. The target IC supply of 3.3 V and the virtual ground potential are produced at the board level using linear regulators, for the second voltage (1.65 V) made from 3.3 V the LDO regulator IC is applied. In similar way, at the board level, the clock signals for modulator and demodulator are produced. The ICL8038 integrated signal generator and two 4047 monostable multivibrators are used for that purpose, fully satisfying non restrictive requirement for those two signals. The 1.2 V from another, small battery is fed to the input dividers attached to the IC under test. The DIP-switch with pull-up resistors used for gain selection, potentiometers for input signal and VCA control, test socket and decoupling capacitors are remaining components of application board. Using the battery supply and on-board generators, it was possible to reduce the connection to line-powered devices to the single one - oscilloscope. This helps to get rid of interferences coming from power-line.

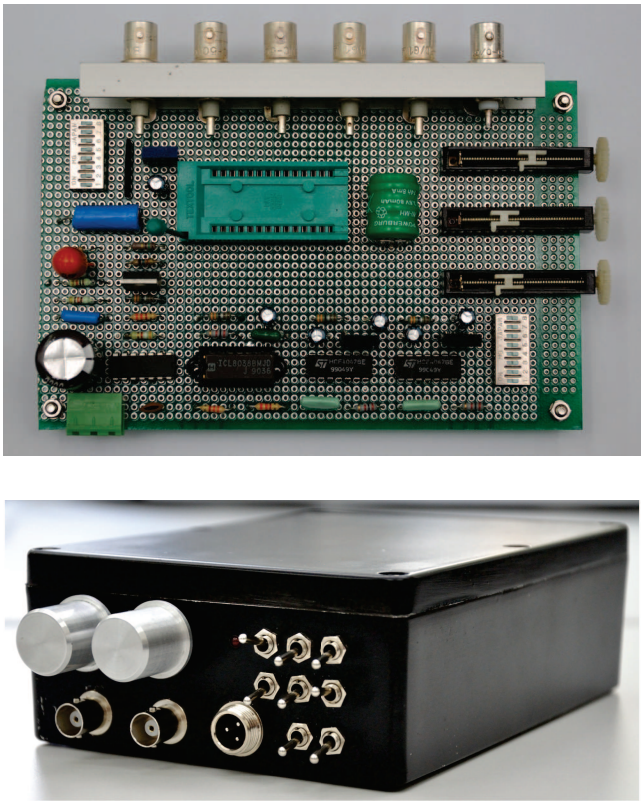

Fig. 13. Designed application board: (top) universal board with components; (bottom) metal enclosure with external terminals

Next important issue was careful shielding of the IC under test, input signal dividers and switches to prevent them from working as receiving antenna. The mentioned 1.2 V battery and resistive divider were used to test the prototype IC with minimum gain setting. For the higher gains it was necessary to provide the low-noise, stable and furthermore adjustable source of DC signal ranging from tens of μV to several mV. The typical value of output voltage from precise voltage reference IC is 1.25, 2.5 or even 5.0 V, the same concerns typical battery cells. Voltage divider applied to decrease it to some hundreds of μV would require large value of one of its resistances, what in turn would negatively influence the noise parameters of such reference voltage source. The next issue is ability of reference voltage regulation - needed to examine the linearity or testing the VCA. In discussed experiment, both problems were overcome by non-typical application of thermocouples. Two thermocouples connected in series in opposite polarity are used to produce the output voltage proportional to the difference of their temperatures. The proportionality coefficient (Seebeck constant) is in order of tens μV. In proposed solution one thermocouple is attached to the heatsink (thermal capacitance) heated up by two power resistors, while the second one is kept in constant temperature. At the beginning of experiments it was intended to put the second junction into thermostat but measurements shown that placing it in large amount of silicon oil in air-conditioned room is good enough. The thermocouples leads are connected together inside the metal box, where the auxiliary voltage divider (made of special low-noise, precise resistors) can be installed to decrease the voltage for measurements for maximum gain setting. Decoupling capacitor can be also attached there. All the connections of described circuit (thermocouples leads and wiring to the board) are made as shielded ones. Without voltage divider the internal resistance of such a non-typical measurement signal source is approx. 40 Ω and the output voltage range is from the tens of μV to approx. 60 mV. It is worth to notice that this signal source also provides the galvanic separation between output (thermocouples) and control circuitry, which is also important for interferences elimination. Measurement results proved the usefulness of presented reference voltage source concept.

During the first chip tests it turned out that demodulator circuits (see II-C) oscillate when they are loaded by significant capacitance, i.e. cable and even oscilloscope probe capacitance. Implicitly voltage follower on the circuit outputs should have been placed, but after chip fabrication it is obviously impossible. Proper circuit operation is achieved by adding external voltage followers which provide cable capacitance decoupling. Placing followers inside IC is undoubtedly one of the issues that should be included in next design.

Figure 13 (bottom) shows metal enclosure for designed application board, which provides shielding and external interferences elimination. Enclosure is equipped with external terminals: BNC sockets, switches and potentiometers.

B. Measurement Results

As it was mentioned in previous section (V-A), external voltage followers are placed on the circuit output to provide capacitance driving. It turned out that even in this configuration it happens that output of the circuit oscillate (when value of input signal is too high). It was assumed that analysing the input signal of demodulator will be more reliable. This is a square wave with k*a amplitude as it was shown in Figure 1. Designed chip has some special pins, which enables monitoring of selected internal signals.

If the amplifier works properly, square wave with amplitude equals to amplified input signal should be observed. In Figures 14 - 16 exemplary oscillograms are shown.

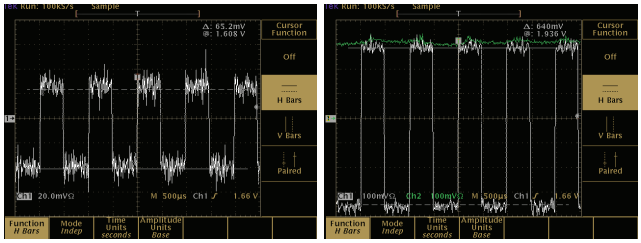

Fig. 14. Chopper amplifier I: (left) input voltage=0.32 mV, k =100, square wave amplitude =32.6 mV; (right) input voltage =0.32 mV, k =1000, square wave amplitude=320 mV

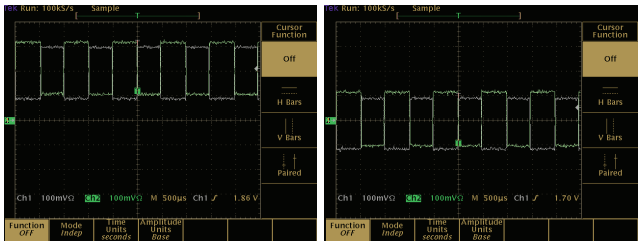

Fig. 15. Chopper amplifier II: (left) common mode voltage control, *vcm*=1.233 V; (right) common mode voltage control, *vcm*=1.395 V

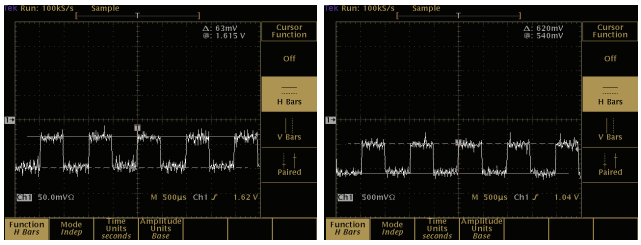

Fig. 16. Chopper amplifier III: (left) linear gain control, *vca*=1.692 V => k=100; (right) linear gain control, *vca*=0.2292 V => k=1000

Figure 14 presents square wave for the 0.32 mV input voltage and gain set to 100/1000. Amplitude of AC signal is proper but some noises are present. Probably these are noises generated in environment around application board - i.e. by power network or measurement equipment. Interferences appear on circuit input and are amplified. For measurement of signals smaller than 0.1 mV better shielding of application board should be used.

Figure 15 shows common mode voltage control described in III-E. Depending on *vcm* signal, CM voltage for PGA input signals assumed different values. This mechanism constitutes protection against amplifier saturation.

Figure 16 presents linear gain control in chopper amplifier III. Depending on *vca* signal, gain value of VCA can be controlled in 1-10 range. In these figures also an unexpected phenomenon can be observed. The DC offset value on circuit output is unnaturally high. Moreover - it depends on gain setting. This issue needs thorough analysis (i.e. device variations analysis using PCM - Process Control Monitors), it should be done during the next design stage.

VI. Conclusion

The simulation shows that chopper amplifier architecture works properly. The only problems concern demodulator circuit, which needs external voltage followers to drive capacitive load. This should be included in the next stage of design.

Presented above oscillograms was measured without metal enclosure shown in Figure 13 (bottom) (it was produced at later stage). In that case measurements for gain >80 dB were impossible (because of external noises), but for <80 dB measured gains matches simulation results.

Very interesting experiment will be lighting the designed chip with THz radiation and observation of amplified detector response. As it was mentioned in IV, there are no previous results of experiment with NMOS detector fabricated in AMS process. This issue will be done in the nearest future.

Acknowledgment

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