A Simple Method for Extraction of Threshold Voltage of FD SOI MOSFETs

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Abstract—**Methods of a MOSFET threshold voltage extraction have been briefly described. A possibility of their application for characterization of a fully-depleted SOI MOSFETs has been discussed. A simple method for SOI MOSFET threshold voltage characterization has been proposed. The concept has been verified based on experimental data obtained for SOI MOSFETs manufactured in ITE.**

Index Terms—**CMOS, Fully-depleted SOI, Threshold voltage, Parameter extraction**

I. Introduction

A threshold voltage extraction is one of the basic steps of the CMOS technology characterization and process design kit (PDK) development [1]. In the case of bulk CMOS technology the threshold voltage dependence on substrate bias, a so-called body-bias effect is used for substrate characterization, e.g. for extraction of substrate doping concentration. Moreover parameters of the threshold voltage dependence on substrate bias are of primary in so-called threshold voltage-based models (e.g. BSIM model family [2], EKV [3]) used for IC design. In the case of SOI CMOS (in particular fully-depleted) circuits and devices the threshold voltage still remains one of the most important device parameters [4]. Its body bias dependence is extensively used for local biasing of IC blocks [5]. It may be also used for the channel conductivity modulation in the sensor applications of FD SOI MOSFETs, e.g. for biomolecule/ion detection [6], or for sub-terahertz radiation detection [7]. However its dependence on substrate bias is different than in the bulk CMOS devices. Moreover the extraction of the threshold voltage dependence on the substrate bias is not a trivial task if a full spectrum of substrate bias from negative to positive values is necessary.

In the presented work a standard model of the FD SOI MOSFET threshold voltage and three standard methods of its extraction have been presented. Also a simple, empirical method for the threshold voltage extraction has been introduced. This approach is predestined for FD SOI MOSFETs. Next, I-V characteristics measured for the FD SOI technology [8] have been used for the threshold voltage extraction. The obtained results have been discussed and compared.

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II. FD SOI CMOS Process Characterization

A Lin-Fossum model [9] of the threshold voltage of the FD SOI MOSFETs comprises accumulation, depletion and inversion conditions. Though simple it may be efficiently used for threshold voltage mapping and for extraction of the process parameters. The model consists of three formulae (1-3) valid for different bias conditions at the bottom Si-SiO_2 interface, namely for accumulation (A), inversion (I) and depletion (D).

$$V_{T,f}^{A} \approx V_{FB,f} + \left(1 + \frac{C_b}{C_{ox,f}}\right) \cdot 2\phi_B - \frac{Q_b}{2C_{ox,f}} \quad (1)$$

$$V_{T,f}^{I} \approx V_{FB,f} + 2\phi_B - \frac{Q_b}{2C_{ox,f}} \quad (2)$$

$$\begin{aligned} V_{T,f}^{D} &\approx V_{T,f}^{A} - \frac{C_b \cdot C_{ox,b}}{C_{ox,f} \cdot (C_b + C_{ox,b} + C_{s,b})}\left(V_{G,b} - V_{G,b}^{A}\right) \\ &\approx V_{T,f}^{I} - \frac{C_b \cdot C_{ox,b}}{C_{ox,f} \cdot (C_b + C_{ox,b} + C_{s,b})}\left(V_{G,b} - V_{G,b}^{I}\right) \end{aligned} \quad (3)$$

where the variables have the meanings mentioned in Table I. $V_{G,b}$ is a substrate (bulk gate) bias. Its values at accumulation/depletion, and depletion/inversion boundaries at the bottom Si/SiO_2 interface are given by (4), (5) respectively.

$$V_{G,b}^{A} \approx V_{FB,b} - \frac{C_b}{C_{ox,b}} \cdot 2\phi_B - \frac{Q_b}{2C_{ox,b}} \quad (4)$$

$$V_{G,b}^{I} \approx V_{FB,b} + \left(1 + \frac{C_{s,b}}{C_{ox,b}}\right) \cdot 2\phi_B - \frac{Q_b}{2C_{ox,b}} \quad (5)$$

Other variables in formulae (1)-(5) and in the Table I have their standard meanings.

The theoretical threshold voltage vs substrate bias dependence is represented by a piece-linear curve. However experimental extraction of a part of this line corresponding to the inversion conditions at the bottom Si/SiO2 interface is not trivial, because the front channel current is masked by the back channel current. In Fig.1 the n-channel MOSFET experimental I_D-V_{Gf} characteristics family is shown [8].

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TABLE I. FD SOI MOSFET THRESHOLD VOLTAGE PARAMETERS

Param.	Definition	Description
$C_{ox,f/b}$	$\varepsilon_{ox}/t_{ox,f/b}$	capacitance of front/bulk gate (per unit area)
$V_{FB,f/b}$	$\phi_{MS,f/b} - q_{f,f/b}/C_{ox,f/b}$	front/bulk-gate flatband voltage (as for bulk MOSFET)
C_b	ε_{Si}/t_b	capacitance of depleted Si film (per unit area)
$C_{s,b}$	$q \cdot N_{s,b}$	capacitance related to fast surface states at bottom Si/SiO_2 interface (per unit area)
q_b	$-q \cdot N_A \cdot t_b$	depleted Si film charge per unit area
ϕ_B	$kT/q \cdot \ln(N_A/n_i)$	Si film Fermi potential;

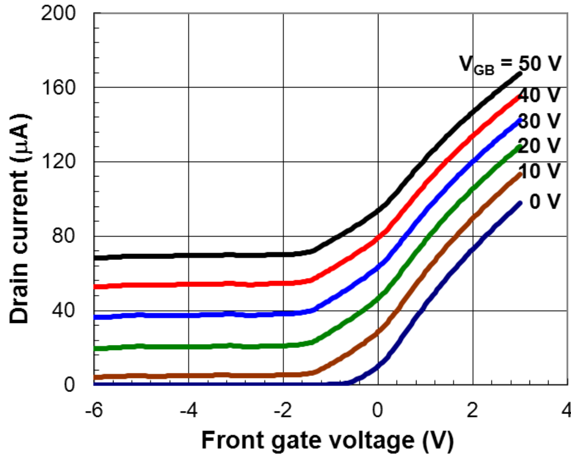

Figure 1. Input I_D-$V_{G,f}$ characteristics of the FD SOI nMOSFET; channel width=20µm, length=2µm, a back channel turning-on along with increasing substrate bias is clearly visible

Below several methods and their potential feasibility for the FD SOI CMOS are briefly discussed. Most of them are widely known and described e.g. in [10, 11].

A. Threshold Voltage Extraction Based on Constant Drain Current

This is a technical threshold voltage measure. I takes into account a total drain current value. The back channel operation in the FD SOI MOSFETs cannot be eliminated. Thus the method may be a priori excluded from further considerations.

B. Threshold Voltage Extraction Based on Linear Extrapolation of I_D-V_G Data

A standard, most frequently used method of threshold voltage extraction is based on transfer I_D-V_G MOSFET characteristics. It is based on intersection point between the V_G axis and the line tangent to the I_D-V_G curve at the point V_G^* where the transconductance g_m reaches maximum. In this approach the I_D-V_G data measured at small drain voltage V_D are used. This method does not account for the back channel operation as well, thus it is not feasible in the case of FD SOI MOSFET characterization. Nevertheless it will be further illustrated based on the experimental data.

C. Threshold Voltage Extraction Based on Linear Extrapolation of $I_D/g_m^{0.5}$-V_G Data

The next method used for extraction of the MOSFET threshold voltages is based on $I_D/g_m^{0.5}$-V_G data [10]. In this method the influence of a non-zero serial source/drain resistances, and of mobility degradation due to transversal gate electrical field are theoretically eliminated. In the case of the effect in the conventional bulk MOSFETs the method leads to linear $I_D/g_m^{0.5}$-V_G dependence. The method will be illustrated based on experimental data in the next section, although it should be mentioned, that it does not meet needs of the FD SOI CMOS characterization.

D. Threshold Voltage Extraction Based on $d(g_m/I_D)/dV_G$-V_G Data

An interesting method for the threshold voltage extraction has been introduced quite recently in [13]. The method consists in evaluation of the $d(g_m/I_D)/dV_G$-V_G characteristics. The threshold voltage corresponds to a maximum of this curve. The method is computationally equivalent to the method based on derivative of gate capacitance approach, thus should be non-sensitive to the effects originating from the charge transport in the channel, e.g. serial resistance, mobility degradation etc. The method has been tested against FD SOI devices. However the tests have not comprise back channel conduction conditions. Moreover it should be noted, that this approach requires high-quality, smooth I_D-V_G measurements, because next these data are twice differentiated. Any disturbances of the original I_D-V_G data may introduce serious errors in the extraction results.

E. Threshold Voltage Extraction Based on Linear Extrapolation of Corrected I_D-V_G Data

This method applies only to the SOI MOSFETs, so an appropriate notation will be used in this subsection. It may be easily noticed, that at the front gate bias corresponding to the accumulation conditions at the top Si-SiO_2 interface ($V_{G,f} < -2$ V) a large drain current is visible (Fig. 1). This current flows along the back channel, and it may be stated, that it depends on the back-gate bias, but depends very weakly on the front-gate bias. If the back-channel current is subtracted from the I_D-$V_{G,f}$ data, then a new, corrected curve family is obtained. It is shown in Fig. 2. In accordance with the Lim-Fossum theory [9] a crowding of the I_D-$V_{G,f}$ curves at the back-gate accumulation ($V_{G,b} < -30$ V) and inversion ($V_{G,b} > 10$ V) ranges may be observed. The overlapping of the characteristics means, that at the inversion or accumulation at the bottom Si/SiO_2 interface the threshold voltage is almost constant with no respect to the back-gate voltage.

III. EXPERIMENTAL

For experimental validation of the extraction methods test devices fabricated in ITE [8] have been used.

A. FD SOI CMOS Technology

The FD SOI CMOS technology has been transferred to ITE within collaboration with Université Catholique de Louvain (UCL) supported by TRIADE project [14]. Main features of

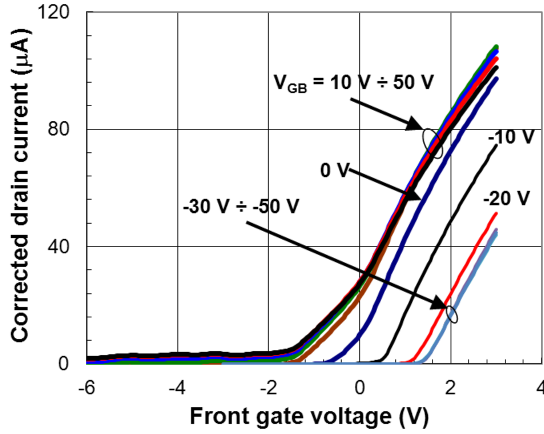

Figure 2. Front channel current-voltage characteristics of the FD SOI nMOSFET after drain current correction.

this process are as follows: supply voltage 3 V, threshold voltage 0.3 V, and min poly-silicon gate width 1.5 µm. The threshold voltage values have been obtained after boron implantations into the channel at energy=20 keV with doses $5\cdot10^{11}$ cm^{-2} (P1 for PMOSFETs) and $8\cdot10^{11}$ cm^{-2} (P2 for NMOSFETs) respectively. The NMOSFETs are operated as enhancement-mode devices, whereas the PMOSFETs are accumulation-mode devices. However it is worthwhile to mention, that in the test structures different types of n- and p-channel MOSFETs are included. Namely, via superposition of two boron doses P1, P2 mentioned above it is possible to get four variants of n- and p-channel MOSFETs with different doping concentrations in the channel (no implant, P1, P2, P1+P2). A schematic cross-section of the FD SOI CMOS pair is shown in Fig. 3 .

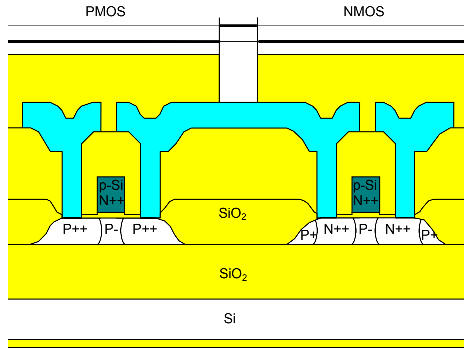

Figure 3. Cross-section of a complementary pair of the FD SOI MOSFETs.

B. *Electrical Measurements*

Measurements of transfer characteristics of transistors have been carried out on semi-automatic probe station using Keithley 236 and 237 source-measure units (SMUs). Front gate and drain pads have been connected with two 236 SMUs, whereas the substrate (i.e. back gate) has been biased through the probe station chuck by the 237 SMU. The MOSFET transfer I_D-$V_{G,f}$ characteristic have been measured for small drain voltage equal to 50 mV.

C. *Threshold Voltage Extraction*

As it has been mentioned earlier, the extraction of threshold voltage based on intersection point between the abscissa and the line tangent to the I_D-$V_{G,f}$ curve gives incorrect values if the bottom interface of FD SOI structure is in inversion. This situation may be observed in Fig. 4 for the back gate voltages ($V_{G,b}$) above 10 V. The threshold voltage extracted this way would be about -3 V for the back-gate voltage $V_{G,b}$ = 50 V, whereas the correct value determined after drain current correction is -0.7 V (Fig. 4).

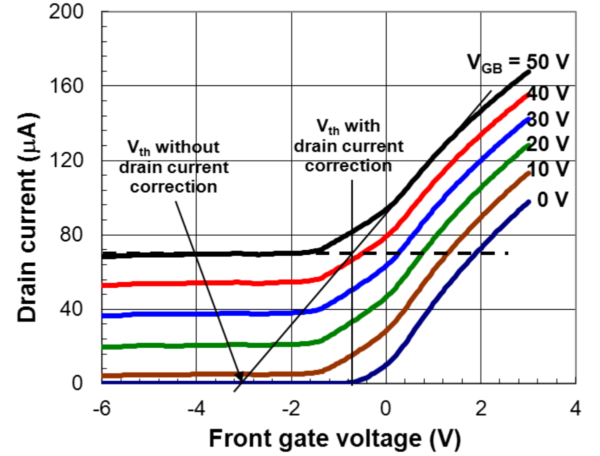

Figure 4. Extraction of the front-gate threshold voltage $V_{th,f}$ using a linear approximation of the I_D-$V_{G,f}$ characteristics; FD SOI nMOSFET; channel width=20µm, length=2µm; inversion at the bottom interface.

The similar effects occur if the method based on linear extrapolation of $I_D/g_m^{0.5}$-V_G data is used (Fig. 5), however the obtained values are closer to the correct ones than in the previous case.

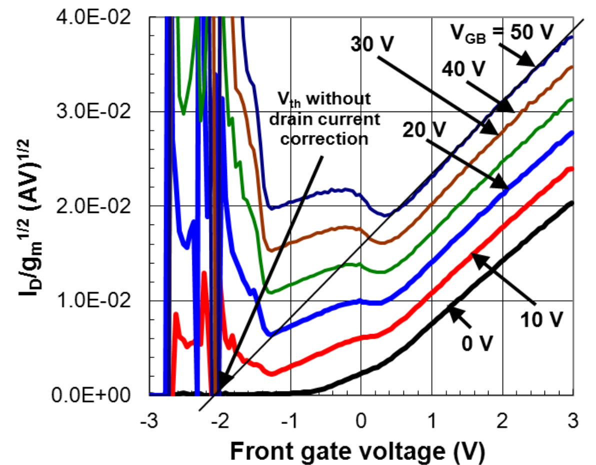

Figure 5. Extraction of the front-gate threshold voltage $V_{th,f}$ using a linear extrapolation of $I_D/g_m^{0.5}$-$V_{G,f}$ data; FD SOI nMOSFET; channel width=20µm, length= 2µm; inversion at the bottom interface.

In the last of the compared methods, the measurements data have been twice differentiated. As a consequence, the analyzed characteristics exhibit significant distortion. In our research we

have observed this effect even in case of bottom interface in accumulation as it is shown in Fig. 6. Determining the exact value of the threshold voltage without smoothing the data is very difficult. In the case of bottom interface bias providing the inversion conditions we have received characteristics that are difficult to interpret (Fig. 7). Extraction of the threshold voltage based on such data is impossible.

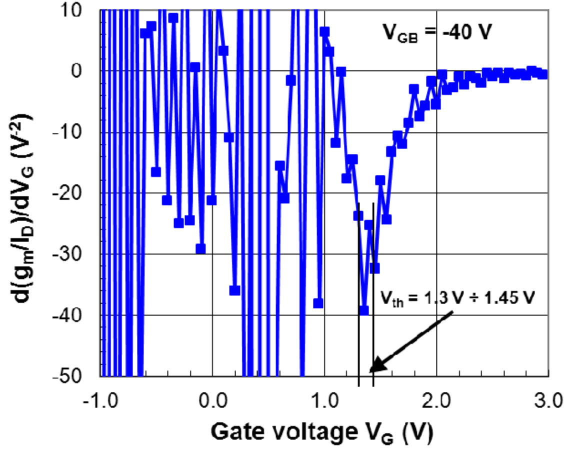

Figure 6. Threshold voltage extraction method based on $d(g_m/I_D)/dV_G$-V_G data in case of bottom interface in accumulation.

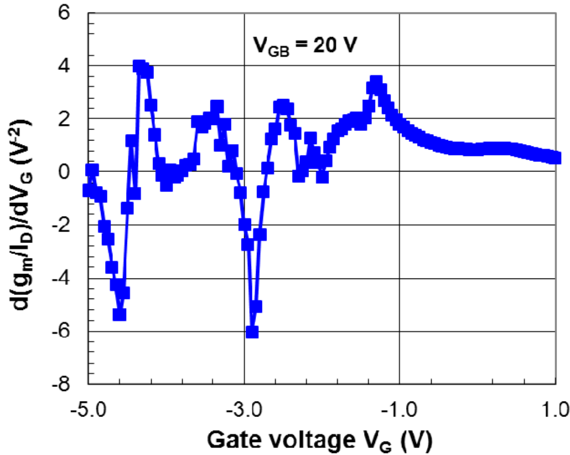

Figure 7. Threshold voltage extraction method based on $d(g_m/I_D)/dV_G$-V_G data in case of bottom interface in inversion.

IV. Discussion of Results

Comparison of the results of the threshold voltage extraction by means of different methods is shown in Fig. 8. It is worth to notice that in the case of accumulation at the bottom interface ($V_{G,b} < -20$ V) all the extracted values are consistent. Completely different behavior is observed when the bottom interface enters the inversion. Under these conditions determining the proper value of the threshold voltage without drain current correction was impossible. After the correction of the drain current the dependence of extracted threshold voltage on substrate bias was in line with expectations.

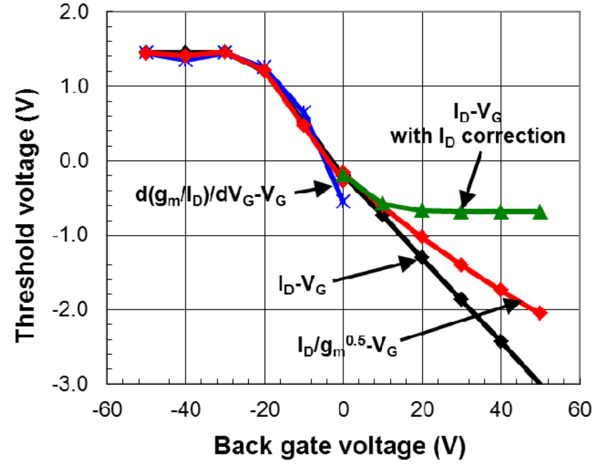

Figure 8. Comparison between I_D-V_G, $I_D/g_m^{0.5}$-V_G , $d(g_m/I_D)/dV_G$-V_G and I_D-V_G with drain current correction methods of the threshold voltage extraction for the FD SOI MOSFETs.

Based on the formula (3) a silicon film thickness may be determined. The results obtained for a set of the n-channel transistors and with different concentration of dopants in the channel region are shown in Fig. 9. As it can be seen the results exhibit a significant spread. In the case of transistors with higher doping concentration (NP2N) we observed higher dispersion of extracted thickness of active layer. In all the cases the obtained results are higher than the technological silicon film thickness measured by means of optical methods. This is due to the large sensitivity of the method on inaccurate determination of the slope of $V_{T,f}^{D}$-$V_{G,b}$ curve in the full depletion range (depletion at the bottom interface).

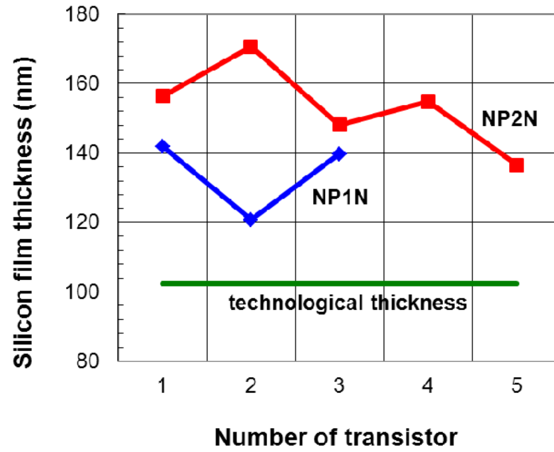

Figure 9. Silicon film thickness extracted for different transistors based on the Lim-Fossum model.

V. Summary

An efficient, empirical method for the threshold voltage of the FD SOI MOSFETs has been presented. The method has been discovered in particular to cope with the problem of extraction of the front-gate threshold voltage for the inversion conditions at the bottom Si-SiO_2 interface. In this range of the

FD SOI MOSFET operation other methods seem to be not fully functional. They have been briefly described in the paper and their shortcomings in the bias range mentioned above have been discussed.

The proposed method is moderately sensitive to the noise of the experimental I_D-$V_{G,f}$ data, because it does not require second-order derivation of the characteristics. Because it allows to reconstruct the $V_{th,f}$-$V_{G,b}$ characteristics in the full range of back-gate bias it provides the user with a tool for evaluation of the Si film thickness. In the paper such calculations have been done for the set of devices manufactured in ITE. The results are not fully consistent with ellipsometry measurements and exhibit a spread. Nevertheless, it is expected that via more accurate electrical measurements for a refined back-gate bias grid the proposed method would give results close to optical characterization results.

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